CLAIM LISTING

This listing of claims will replace all prior versions, and listings of claims in the application:

IN THE CLAIMS

1. (Currently Amended) A programmable serializing data path comprises:

programmable timing circuit operably coupled to generate a first plurality of timing signals when the width of parallel input data is of a first multiple and to generate a second plurality of timing signals when the width of the parallel input data is of a second multiple; and

parallel to serial module operably coupled to convert the parallel input data into serial output data based on the first or second plurality of timing signals.

2. (Currently Amended) The programmable serializing data path of claim 1, wherein the programmable timing circuit further comprises:

a phase locked loop operably coupled to generate a serial data clock from a reference clock;

a clock divider module operably coupled to divide the serial data clock into an intermediate data clock; and

programmable clock divider module operably coupled to divide the intermediate data clock into a first parallel data clock when a clock select signal is in a first state and to divide the intermediate data clock into a second parallel data clock when the clock select signal is in a second state, wherein the clock select signal is in the first state when the width of parallel input data is of the first multiple and is in the second state when the width of the parallel input data is of the second multiple, wherein the first plurality of timing signals includes the serial data clock, the intermediate data clock, and the first parallel data clock, and wherein the second plurality of timing signals includes the serial data clock, the intermediate data clock, and the second parallel data clock.

3. (Original) The programmable serializing data path of claim 2, wherein the programmable clock divider module further comprises:

a first flip-flop having an input, an output, and a clock input;

a second flip-flop having an input, an output, and a clock input, wherein the input of the second flip-flop is coupled to the output of the first flip-flop;

a third flip-flop having an input, an output, and a clock input, wherein the clock inputs of the first, second, and third flip-flops are operably coupled to receive the intermediate data clock;

a multiplexer having a first input, a second input, an output, and a control input, wherein the control input is operably coupled to receive the clock select signal, the first input of the multiplexer is operably coupled to receive a fixed logic signal, the second input of the multiplexer is operably coupled to the output of the second flip-flop, and the output of the multiplexer is operably coupled to the input of the third flip-flop; and

a NOR gate having a first input, a second input, and an output, wherein the first input of the NOR gate is operably coupled to the output of the second flip-flop, the second input of the NOR gate is operably coupled to the output of the third flip-flop, and the output of the NOR gate is operably coupled to the input of the first flip-flop, wherein the outputs of the first, second, and third flip-flops provide the first or second parallel data clock.

4. (Original) The programmable serializing data path of claim 3, wherein the parallel to serial module further comprises:

first multiplexing module operably coupled to convert the parallel input data into first intermediate data based on the first or second parallel data clock;

second multiplexing module operably coupled to convert the first intermediate data into second intermediate data based on the intermediate data clock; and

third multiplexing module operably coupled to convert the second intermediate data into the serial output data based on the serial data clock.

5. (Original) The programmable serializing data path of claim 4, wherein the first multiplexing module comprises:

a plurality of multiplexers, wherein each of the plurality of multiplexers includes a multi-bit input, a single-bit output, and a multi-bit control input, wherein the multi-bit control input is operably coupled to receive the first or second parallel data clock, wherein the parallel input data is divided into sections, where a number of bits in each of the sections of the parallel input data corresponds to a number of multiplexers in the plurality of multiplexers, wherein the multi-bit input of each of the plurality of multiplexers is operably coupled to receive a corresponding bit from each of the sections of the parallel input data, and wherein each of the plurality of multiplexers outputs, via the single-bit output, one of the corresponding bits of one of the sections of the parallel input data at each state transition of the first or second parallel data clock.

6. (Original) The programmable serializing data path of claim 5, wherein the programmable timing circuit further functions to generate:

a three bit, five state parallel data clock as the first parallel data clock when the parallel input data is twenty bits wide;

a three bit, four state parallel data clock as the second parallel data clock when the parallel input data is sixteen bits wide;

a four bit, ten state parallel data clock as the first parallel data clock when the parallel input data is forty bits wide; and

a four bit, eight state parallel data clock as the second parallel data clock when the parallel input data is thirty-two bits wide.

7. (Original) The programmable serializing data path of claim 5, wherein the second multiplexing module comprises:

a first multiplexer having a multi-bit input, a single-bit output, and a control input, wherein the multi-bit input of the first multiplexer is operably coupled to receive outputs of a first set of the plurality of multiplexers, wherein the control input of the first multiplexer is operably coupled to receive the intermediate data clock, and wherein the first multiplexer outputs, via the single-bit output of the first multiplexer, a corresponding one of the outputs of the first set of the plurality of multiplexers based on the intermediate data clock; and

a second multiplexer having a multi-bit input, a single-bit output, and a control input, wherein the multi-bit input of the second multiplexer is operably coupled to receive outputs of a second set of the plurality of multiplexers, wherein the control input of the second multiplexer is operably coupled to receive the intermediate data clock, and wherein the second multiplexer outputs, via the single-bit output of the second multiplexer, a corresponding one of the outputs of the second set of the plurality of multiplexers based on the intermediate data clock.

8. (Original) The programmable serializing data path of claim 7, wherein the parallel to serial module further comprises:

a first input latch operably coupled to temporarily store the parallel input data and to provide the parallel input data to the plurality of multiplexers in a synchronized manner;

an output latch operably coupled to temporarily store the outputs of the plurality of multiplexers;

a second input latch operably coupled to the output latch and to temporarily store the outputs of the first set of the plurality of multiplexers, wherein the second input latch provides the outputs of the first set of the plurality of multiplexers to the first multiplexer in the synchronized manner; and

a third input latch operably coupled to the output latch and to temporarily store the outputs of the second set of the plurality of multiplexers, wherein the third input latch provides the outputs of the second set of the plurality of multiplexers to the second multiplexer in the synchronized manner.

9. (Currently Amended) A programmable logic device comprises:

a transmit physical media attachment module operably coupled to convert parallel input data into serial output data;

a receive physical media attachment module operably coupled to convert receive serial data into receive parallel data;

a transmit physical coding sublayer module operably coupled to convert transmit data words into the parallel input data;

a receive physical coding sublayer module operably coupled to convert the receive parallel data into receive data words; and

programmable logic fabric operably coupled to provide the transmit data words to the transmit physical coding sublayer module to receive the receive data words from the receive physical coding sublayer module, wherein the transmit physical media attachment module includes:

a programmable serializing data path operably coupled to convert the parallel input data into the serial output data; and

a line driver operably coupled to drive the serial output data onto a transmission line coupled to the programmable logic device, wherein the programmable serializing data path includes:

programmable timing circuit operably coupled to generate a first plurality of timing signals when the width of parallel input data is of a first multiple and to generate a second plurality of timing signals when the width of the

parallel input data is of a second multiple; and

parallel to serial module operably coupled to convert the parallel input data into serial output data based on the first or second plurality of timing signals.

10. (Original) The programmable logic device of claim 9, wherein the programmable timing circuit further comprises:

a phase locked loop operably coupled to generate a serial data clock from a reference clock;

a clock divider module operably coupled to divide the serial data clock into an intermediate data clock; and

programmable clock divider module operably coupled to divide the intermediate data clock into a first parallel data clock when a clock select signal is in a first state and to divide the intermediate data clock into a second parallel data clock when the clock select signal is in a second state, wherein the clock select signal is in the first state when width of parallel input data is of the first multiple and is in the second state when the width of the parallel input data is of the second multiple, wherein the first plurality of timing signals includes the serial data clock, the intermediate data clock, and the first parallel data clock, and wherein the second plurality of timing signals includes the serial data clock, the intermediate data clock, and the second parallel data clock.

11. (Original) The programmable logic device of claim 10, wherein the programmable clock divider module further comprises:

a first flip-flop having an input, an output, and a clock input;

a second flip-flop having an input, an output, and a clock input, wherein the input of the second flip-flop is coupled to the output of the first flip-flop;

a third flip-flop having an input, an output, and a clock input, wherein the clock inputs of the first, second, and third flip-flops are operably coupled to receive the intermediate data clock;

a multiplexer having a first input, a second input, an output, and a control input, wherein the control input is operably coupled to receive the clock select signal, the first input of the multiplexer is operably coupled to receive a fixed logic signal, the second input of the multiplexer is operably coupled to the output of the second flip-flop, and the output of the multiplexer is operably coupled to the input of the third flip-flop; and

a NOR gate having a first input, a second input, and an output, wherein the first input of the NOR gate is operably coupled to the output of the second flip-flop, the second input of the NOR gate is operably coupled to the output of the third flip-flop, and the output of the NOR gate is operably coupled to the input of the first flip-flop, wherein the outputs of the first, second, and third flip-flops provide the first or second parallel data clock.

12. (Original) The programmable logic device of claim 11, wherein the parallel to serial module further comprises:

first multiplexing module operably coupled to convert the parallel input data into first intermediate data based on the first or second parallel data clock;

second multiplexing module operably coupled to convert the first intermediate data into second intermediate data based on the intermediate data clock; and

third multiplexing module operably coupled to convert the second intermediate data into the serial output data based on the serial data clock.

13. (Original) The programmable logic device of claim 12, wherein the first multiplexing module comprises:

a plurality of multiplexers, wherein each of the plurality of multiplexers includes a multi-bit input, a single-bit output, and a multi-bit control input, wherein the multi-bit control input is operably coupled to receive the first or second parallel data clock, wherein the parallel input data is divided into sections, where a number of bits in each of the sections of the parallel input data corresponds to a number of multiplexers in the plurality of multiplexers, wherein the multi-bit input of each of the plurality of multiplexers is operably coupled to receive a corresponding bit from each of the sections of the parallel input data, and wherein each of the plurality of multiplexers outputs, via the single-bit output, one of the corresponding bits of one of the sections of the parallel input data at each state transition of the first or second parallel data clock.

14. (Original) The programmable logic device of claim 13, wherein the programmable timing circuit further functions to generate:

a three bit, five state parallel data clock as the first parallel data clock when the parallel input data is twenty bits wide;

a three bit, four state parallel data clock as the second parallel data clock when the parallel input data is sixteen bits wide;

a four bit, ten state parallel data clock as the first parallel data clock when the parallel input data is forty bits wide; and

a four bit, eight state parallel data clock as the second parallel data clock when the parallel input data is thirty-two bits wide.

15. (Original) The programmable logic device of claim 13, wherein the second multiplexing module comprises:

a first multiplexer having a multi-bit input, a single-bit output, and a control input, wherein the multi-bit input of the first multiplexer is operably coupled to receive outputs of a first set of the plurality of multiplexers, wherein the control input of the first multiplexer is operably coupled to receive the intermediate data clock, and wherein the first multiplexer outputs, via the single-bit output of the first multiplexer, a corresponding one of the outputs of the first set of the plurality of multiplexers based on the intermediate data clock; and

a second multiplexer having a multi-bit input, a single-bit output, and a control input, wherein the multi-bit input of the second multiplexer is operably coupled to receive outputs of a second set of the plurality of multiplexers, wherein the control input of the second multiplexer is operably coupled to receive the intermediate data clock, and wherein the second multiplexer outputs, via the single-bit output of the second multiplexer, a corresponding one of the outputs of the second set of the plurality of multiplexers based on the intermediate data clock.

16. (Original) The programmable logic device of claim 15, wherein the parallel to serial module further comprises:

a first input latch operably coupled to temporarily store the parallel input data and to provide the parallel input data to the plurality of multiplexers in a synchronized manner;

an output latch operably coupled to temporarily store the outputs of the plurality of multiplexers;

a second input latch operably coupled to the output latch and to temporarily store the outputs of the first set of the plurality of multiplexers, wherein the second input latch provides the outputs of the first set of the plurality of multiplexers to the first multiplexer in the synchronized manner; and

a third input latch operably coupled to the output latch and to temporarily store the outputs of the second set of the plurality of multiplexers, wherein the third input latch provides the outputs of the second set of the plurality of multiplexers to the second multiplexer in the synchronized manner.

17. (Withdrawn) A method for programmable serializing of parallel data, the method comprises:

receiving the parallel data;

obtaining a data width of the parallel data, wherein the data width is of a first multiple or a second multiple;

obtaining a desired serial data output rate;

generating a multiple state control sequence based on the data width of the parallel data and the desired serial data output rate; and

converting the parallel data into serial data in accordance with the multiple state control sequence.

18. (Withdrawn) The method of claim 17, wherein the obtaining the data width of the parallel data comprises at least one of:

receiving an input selection of the data width; and

automatically determining the data width based on the receiving of the parallel data.

19. (Withdrawn) The method of claim 17, wherein the generating the multiple state control sequence further comprises:

generating a serial data clock having a rate corresponding to the desired serial data output rate;

generating a first set of control signals from the serial data clock when the data width is of a first multiple, wherein the serial data clock and the first set of control signals constitutes the multiple state control sequence; and

generating a second set of control signals from the serial data clock when the data width is of a second multiple, wherein the serial data clock, the intermediate data clock, and the second set of control signals constitutes the multiple state control sequence.

20. (Withdrawn) The method of claim 17, wherein the generating the multiple state control sequence further comprises:

generating a serial data clock having a rate corresponding to the desired serial data output rate;

dividing the serial data clock into an intermediate data clock;

generating a first set of control signals from the intermediate data clock when the data width is of a first multiple, wherein the serial data clock, the intermediate data clock, and the first set of control signals constitutes the multiple state control sequence; and

generating a second set of control signals from the intermediate data clock when the data width is of a second multiple, wherein the serial data clock, the intermediate data clock, and the second set of control signals constitutes the multiple state control sequence.

21. (Withdrawn) The method of claim 20, wherein the generating the first and second set of control signals further comprises generating:

a three bit, five state parallel data clock as the first set of control signals when the parallel data is twenty bits wide;

a three bit, four state parallel data clock as the second set of control signals when the parallel data is sixteen bits wide;

a four bit, ten state parallel data clock as the first set of control signals when the parallel data is forty bits wide; and

a four bit, eight state parallel data clock as the second set of control signals when the parallel data is thirty-two bits wide.

22. (Withdrawn) The method of claim 21, wherein the converting the parallel data into serial data further comprises:

when the width of the parallel data is twenty:

selecting bits of the parallel data per sequencing of the three bit, five state parallel data clock to produce a first set of intermediate bits;

selecting two bits of the first set of intermediate bits per cycle of the intermediate data clock to produce two selected bits; and

selecting one of the two selected bits per cycle of the serial data clock to produce the serial data;

when the width of the parallel data is sixteen:

selecting bits of the parallel data per sequencing of the three bit, four state parallel data clock to produce a second set of intermediate bits;

selecting two bits of the second set of intermediate bits per cycle of the intermediate data clock to produce the two selected bits; and

selecting one of the two selected bits per cycle of the serial data clock to produce the serial data.

23. (Withdrawn) A programmable serializing data path comprises:

processing module; and

memory operably coupled to the processing module, wherein the memory stores operational instructions that cause the processing module to:

receive the parallel data;

obtain a data width of the parallel data, wherein the data width is of a first multiple or a second multiple;

obtain a desired serial data output rate;

generate a multiple state control sequence based on the data width of the parallel data and the desired serial data output rate; and

convert the parallel data into serial data in accordance with the multiple state control sequence.

24. (Withdrawn) The programmable serializing data path of claim 23, wherein the memory further comprises operational instructions that cause the processing module to obtain the data width of the parallel data by at least one of:

receiving an input selection of the data width; and

automatically determining the data width based on the receiving of the parallel data.

25. (Withdrawn) The programmable serializing data path of claim 23, wherein the memory further comprises operational instructions that cause the processing module to generate the multiple state control sequence by:

generating a serial data clock having a rate corresponding to the desired serial data output rate;

generating a first set of control signals from the serial data clock when the data width is of a first multiple, wherein the serial data clock and the first set of control signals constitutes the multiple state control sequence; and

generating a second set of control signals from the serial data clock when the data width is of a second multiple, wherein the serial data clock, the intermediate data clock, and the second set of control signals constitutes the multiple state control sequence.

26. (Withdrawn) The programmable serializing data path of claim 23, wherein the memory further comprises operational instructions that cause the processing module to generate the multiple state control sequence by:

generating a serial data clock having a rate corresponding to the desired serial data output rate;

dividing the serial data clock into an intermediate data clock;

generating a first set of control signals from the intermediate data clock when the data width is of a first multiple, wherein the serial data clock, the intermediate data clock, and the first set of control signals constitutes the multiple state control sequence; and

generating a second set of control signals from the intermediate data clock when the data width is of a second multiple, wherein the serial data clock, the intermediate data clock, and the second set of control signals constitutes the multiple state control sequence.

27. (Withdrawn) The programmable serializing data path of claim 26, wherein the memory further comprises operational instructions that cause the processing module to generate the first and second set of control signals by generating:

a three bit, five state parallel data clock as the first set of control signals when the parallel data is twenty bits wide;

a three bit, four state parallel data clock as the second set of control signals when the parallel data is sixteen bits wide;

a four bit, ten state parallel data clock as the first set of control signals when the parallel data is forty bits wide; and

a four bit, eight state parallel data clock as the second set of control signals when the parallel data is thirty-two bits wide.

28. (Withdrawn) The programmable serializing data path of claim 27, wherein the memory further comprises operational instructions that cause the processing module to convert the parallel data into serial data by:

when the width of the parallel data is twenty:

selecting bits of the parallel data per sequencing of the three bit, five state parallel data clock to produce a first set of intermediate bits;

selecting two bits of the first set of intermediate bits per cycle of the intermediate data clock to produce two selected bits; and

selecting one of the two selected bits per cycle of the serial data clock to produce the serial data;

when the width of the parallel data is sixteen:

selecting bits of the parallel data per sequencing of the three bit, four state parallel data clock to produce a second set of intermediate bits;

selecting two bits of the second set of intermediate bits per cycle of the intermediate data clock to produce the two selected bits; and

selecting one of the two selected bits per cycle of the serial data clock to produce the serial data.

29. (Withdrawn) A programmable logic device comprises:

a transmit physical media attachment module operably coupled to convert parallel input data into serial output data;

a receive physical media attachment module operably coupled to convert receive serial data into receive parallel data;

a transmit physical coding sublayer module operably coupled to convert transmit data words into the parallel input data;

a receive physical coding sublayer module operably coupled to convert the receive parallel data into receive data words; and

programmable logic fabric operably coupled to provide the transmit data words to the transmit physical coding sublayer module to receive the receive data words from the receive physical coding sublayer module, wherein the transmit physical media attachment module includes:

a programmable serializing data path operably coupled to convert the parallel input data into the serial output data; and

a line driver operably coupled to drive the serial output data onto a transmission line coupled to the programmable logic device, wherein the programmable serializing data path includes:

processing module; and

memory operably coupled to the processing module, wherein the

memory stores operational instructions that cause the processing module to:

receive the parallel input data;

obtain a data width of the parallel input data, wherein the data width is of a first multiple or a second multiple;

obtain a desired serial data output rate;

generate a multiple state control sequence based on the data width of the parallel input data and the desired serial data output rate; and

convert the parallel input data into serial data in accordance with the multiple state control sequence.

30. (Withdrawn) The programmable logic device of claim 29, wherein the memory further comprises operational instructions that cause the processing module to obtain the data width of the parallel input data by at least one of:

receiving an input selection of the data width; and

automatically determining the data width based on the receiving of the parallel input data.

31. (Withdrawn) The programmable logic device of claim 29, wherein the memory further comprises operational instructions that cause the processing module to generate the multiple state control sequence by:

generating a serial data clock having a rate corresponding to the desired serial data output rate;

generating a first set of control signals from the serial data clock when the data width

is of a first multiple, wherein the serial data clock, the intermediate data clock, and the first set of control signals constitutes the multiple state control sequence; and

generating a second set of control signals from the serial data clock when the data width is of a second multiple, wherein the serial data clock and the second set of control signals constitutes the multiple state control sequence.

32. (Withdrawn) The programmable logic device of claim 29, wherein the memory further comprises operational instructions that cause the processing module to generate the multiple state control sequence by:

generating a serial data clock having a rate corresponding to the desired serial data output rate;

dividing the serial data clock into an intermediate data clock;

generating a first set of control signals from the intermediate data clock when the data width is of a first multiple, wherein the serial data clock, the intermediate data clock, and the first set of control signals constitutes the multiple state control sequence; and

generating a second set of control signals from the intermediate data clock when the data width is of a second multiple, wherein the serial data clock, the intermediate data clock, and the second set of control signals constitutes the multiple state control sequence.

33. (Withdrawn) The programmable logic device of claim 32, wherein the memory further comprises operational instructions that cause the processing module to generate the first and second set of control signals by generating:

a three bit, five state parallel data clock as the first set of control signals when the parallel input data is twenty bits wide;

a three bit, four state parallel data clock as the second set of control signals when the

parallel input data is sixteen bits wide;

a four bit, ten state parallel data clock as the first set of control signals when the parallel input data is forty bits wide; and

a four bit, eight state parallel data clock as the second set of control signals when the parallel input data is thirty-two bits wide.

34. (Withdrawn) The programmable logic device of claim 33, wherein the memory further comprises operational instructions that cause the processing module to convert the parallel input data into serial data by:

when the width of the parallel input data is twenty:

selecting bits of the parallel input data per sequencing of the three bit, five state parallel data clock to produce a first set of intermediate bits;

selecting two bits of the first set of intermediate bits per cycle of the intermediate data clock to produce two selected bits; and

selecting one of the two selected bits per cycle of the serial data clock to produce the serial data;

when the width of the parallel input data is sixteen:

selecting bits of the parallel input data per sequencing of the three bit, four state parallel data clock to produce a second set of intermediate bits;

selecting two bits of the second set of intermediate bits per cycle of the intermediate data clock to produce the two selected bits; and

selecting one of the two selected bits per cycle of the serial data clock to produce the serial data.

35. (Currently Amended) A programmable timing circuit comprises:

a phase locked loop operably coupled to generate a serial data clock from a reference clock; and

a programmable clock divider module operably coupled to divide the serial data clock into a first parallel data clock when a clock select signal is in a first state and to divide the serial data clock into a second parallel data clock when the clock select signal is in a second state, wherein the first state of the clock select signal corresponds to a first multiple of states of the first parallel data clock and wherein the second state of the clock select signal corresponds to a second multiple of states of the second parallel data clock;

wherein the first state of the clock select signal further corresponds to the width of parallel input data being of a first multiple and

wherein the second state of the clock select signal further corresponds to the width of the parallel input data being of a second multiple.

36. (Original) The programmable timing circuit of claim 35, wherein the programmable clock divider module further comprises:

a clock divider module operably coupled to divide the serial data clock into an intermediate data clock, wherein the intermediate clock is used to produce the first or the second parallel data clock.

37. (Original) The programmable timing circuit of claim 36, wherein the programmable clock divider module further comprises:

a first flip-flop having an input, an output, and a clock input;

a second flip-flop having an input, an output, and a clock input, wherein the input of the second flip-flop is coupled to the output of the first flip-flop;

a third flip-flop having an input, an output, and a clock input, wherein the clock inputs of the first, second, and third flip-flops are operably coupled to receive the intermediate data clock;

a multiplexer having a first input, a second input, an output, and a control input, wherein the control input is operably coupled to receive the clock select signal, the first input of the multiplexer is operably coupled to receive a fixed logic signal, the second input of the multiplexer is operably coupled to the output of the second flip-flop, and the output of the multiplexer is operably coupled to the input of the third flip-flop; and

a NOR gate having a first input, a second input, and an output, wherein the first input of the NOR gate is operably coupled to the output of the second flip-flop, the second input of the NOR gate is operably coupled to the output of the third flip-flop, and the output of the NOR gate is operably coupled to the input of the first flip-flop, wherein the outputs of the first, second, and third flip-flops provide the first or second parallel data clock.